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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,764	11/03/2003	Albert Sun	MXIC 1520-1	4234

22470 7590 11/27/2007
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EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	

MAIL DATE	DELIVERY MODE
11/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/699,764	SUN ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 10/30/2007.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/30/2007 has been entered and carefully considered.

2. None of claims are amended, cancelled or newly added. Therefore, claims 1-32 are currently pending in this application.

3. The IDS filed on 10/30/2007 has been entered and carefully considered.

4. Applicant's arguments filed on 10/30/2007 have been fully considered but they are not persuasive.

5. The rejection of claims 1-32 as in the previous office action is respectfully maintained and reiterated below for Applicant's convenience.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-2, 4-6, 11-15, 17, 20-21, 23-25 and 28-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Ikeda et al. (USPN: 2003/0184339) hereinafter, Ikeda.

As per claim 1, Ikeda teaches an integrated circuit (i.e. the system LSI 10 in Fig. 1) comprising: an input port (i.e. shown in Fig. 1 connecting device 2 and 15) by which data is received from a source (i.e. the DRAM 2 in Fig. 1) external to the integrated circuit (e.g. see Fig. 1); a configurable logic array (i.e. the Offchip FPGA 14 in Fig. 1) having a programmable configuration defined by configuration data stored in electrically programmable configuration points within the configurable logic array; memory (i.e. the RAM or ROM for storing the execution program 3 shown in Fig. 1) storing instructions for a mission function for the integrated circuit, storing instructions for a configuration load function used to receive configuration data via said input port, and storing instructions for a configuration function used to transfer the configuration data to the programmable configuration points within the configurable logic array; and a processor (i.e. the RISC processor 11 in Fig. 1) coupled to the memory which fetches and executes said instructions from the memory (e.g. see paragraphs [0051]-[0052] and Fig. 1).

As per claims 2 and 4, Ikeda teaches the claimed invention as described above and furthermore, Ikeda teaches that the memory (i.e. the ROM for storing the execution program 3 shown in Fig. 1) comprises a nonvolatile read-only memory (i.e. the ROM) (e.g. see Fig. 1).

As per claims 5 and 6, Ikeda teaches the claimed invention as described above. In order to load/receive data from external device(s) and transferring the data within the FPGA, the load function/instruction and the transfer function/instruction has to be stored in the memory so the processor can execute/run it.

As per claims 11-13, Ikeda teaches the claimed invention as described above and furthermore, Ikeda teaches that the electrically programmable configuration points comprise floating gate memory cells, nonvolatile, charge programmable memory cells and nonvolatile, programmable memory cells (i.e. the offchip FPGA 14 in Fig. 1).

As per claims 14, Ikeda teaches the claimed invention as described above and furthermore, Ikeda teaches that the integrated circuit further comprises an interface (i.e. the combination of 17, 18, 20 and 21 in Fig. 1) between the processor (i.e. 11 in Fig. 1) and the configurable logic array (i.e. 14 in Fig. 1) supporting the configuration load function (e.g. see Fig. 1).

As per claims 15, Ikeda teaches the claimed invention as described above and furthermore, Ikeda teaches that the memory (i.e. the RAM or ROM for storing the execution program 3 shown in Fig. 1) stores instruction for an in-circuit programming function (e.g. see Fig. 1).

As per claims 17, Ikeda teaches the claimed invention as described above and furthermore, Ikeda teaches that the processor comprises a configurable logic array (i.e. the offchip FPGA 14 in Fig. 1) configured to execute the instructions (e.g. see Fig. 1).

As per claims 20-21, 23-25 and 28-30, see arguments with respect to the rejection of claims 1-2, 4-6 and 11-13, respectively. Claims 20-21, 23-25 and 28-30 are

also rejected based on the same rationale as the rejection of claims 1-2, 4-6 and 11-13, respectively.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda in view of Hsu et al. (USPN: 5,359,570) hereinafter, Hsu.

As per claims 3 and 22, Ikeda teaches that the memory comprises a nonvolatile read-only memory (i.e. the ROM for storing the execution program 3 shown in Fig. 1). However, Ikeda does not teach that the memory comprises a floating gate memory device. Hsu, on the other hand, teaches that floating gate memory devices have the advantage over using the ROM that they can be programmed and erased, electrically, thereby, exhibiting the advantages of ROM memory, i.e., low power consumption and faster access, along with the writeability of magnetic medium. In addition, as integrated circuit fabrication scale increases, greater density can be achieved. Therefore, it would have been obvious to combine Hsu and Ikeda for the benefits described above.

7. Claims 7-8, 18-19 and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda in view of Sun et al. (USPN: 6,401,221) hereinafter, Sun.

As per claims 7 and 8, Ikeda teaches that the claimed invention as described above, but failed to teach the watchdog timer as claimed. Sun, however, discloses a watchdog timer coupled to the CPU (i.e. 122 in Fig. 1), a configuration function that includes using a timer to generate a reset on a response to an error, upon the initialization event, reexecuting the configuration load and configuration function (column 4, lines 15-19). Ikeda and Sun et al. are analogous art because they are from the same field of endeavor, an in circuit programming system that can run downloaded code and reset the system when necessary. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate a watchdog timer and the functions that come with the timer. The suggestion for doing so would have been the ability to reset the system when an error occurs. Therefore, it would have been obvious to combine Sun and Ikeda for the benefit of resetting the system to obtain the invention as specified in claims 7 and 8.

As per claims 18-19 and 31-32, see arguments with respect to the rejection of claim 8. Claims 18-19 and 31-32 are also rejected based on the same rationale as the rejection of claim 8.

8. Claims 9 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda in view of Sun et al. (USPN: 5,901,330) hereinafter, Sun2.

As per claims 9 and 26, Ikeda teaches that the claimed invention as described above, but failed to teach that the configuration load function includes receiving encrypted configuration data via an input port on the integrated circuit, and decrypting

the configuration data. Sun2, however, discloses that the configuration load function includes receiving encrypted configuration data via the input port and then decrypting the configuration data (column 13, lines 59-66). Ikeda and Sun2 are analogous art because they are from the same field of endeavor, an in circuit programming system that can run downloaded code and reset the system when necessary. At the time of the invention it would have been obvious to a person of ordinary skill in the art to encrypt the incoming data and then decrypt the data. The suggestion for doing so would have been system security. Therefore, it would have been obvious to combine Sun2 and Ikeda for the benefit of security to obtain the invention as specified in claims 9. The examiner notes that the in-circuit programming and the configuration load function perform the same function and are therefore not dissimilar enough to differentiate given the known definitions of the two terms.

9. Claims 10 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda in view of Lawman (USPN: 6,028,445).

As per claim 10 and 27, Ikeda teaches that the claimed invention as described above, but failed to teach that the configuration load function includes receiving compressed configuration data via an input port on the integrated circuit, and uncompressing the configuration data. Lawman, however, discloses a configuration load function that includes receiving compressed configuration data via an input port and then decompressing the data (column 8, lines 12-33). Ikeda and Lawman are analogous ad because both deal with downloading data in a compressed format to a

programmable device. At the time of the invention it would have been obvious to a person of ordinary skill in the art to allow the configuration load function to receive compressed data and to decompress it. The suggestion for doing so would have been to save time and bandwidth. Therefore, it would have been obvious to combine Lawman and Ikeda for the benefit of time and bandwidth savings to obtain the invention as specified in claims 10.

10. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda in view of Akao et al. (USPN: 5,900,008) hereinafter, Akao.

As per claim 16, Ikeda teaches that the claimed invention as described above, but failed to teach that the memory include a protected memory array storing instructions for a first configuration load function, a second memory array storing instructions for a second configuration load function, the first memory array protected from alteration by a programming function, and the second memory accessible to be written/modified by the programming function.

Akao, on the other hand, teaches the memory include a protected memory array storing instructions for a first configuration load function, a second memory array storing instructions for a second configuration load function, the first memory array protected from alteration by a programming function, and the second memory accessible to be written/modified by the programming function (e.g. see the Abstract). Ikeda and Akao are analogous art because they are from a similar problem solving area, processing systems that employ program areas and protection for some of the areas. At the time of the invention it would have been obvious to a person of ordinary skill in the ad to add a

protected memory area. The suggestion for doing so would have been protect the data from accidental or malicious overwrites/deletes. Therefore, it would have been obvious to combine Akao and Ikeda for the benefit of data protection to obtain the invention as specified in claim 16. The examiner notes that Akao does not expressly state protecting the first configuration load function or not protecting the second configuration load function, but that combining Akao and Ikeda would give anyone with skill in the art motivation to protect one of the configuration load functions.

Remarks

11. As to remark, Applicant asserted:

(a) The Examiner has mistakenly characterized the "data" supplied from the matrix to the FPGA in paragraph [0052] as "configuration data" for the FPGA. In fact, as can be seen in lines 2-4 of paragraph [0052], the "data" is working data that is supplied from the matrix 20, processed by the FPGA, and that processed result in then returned to the matrix 20. This processing of working data by the FPGA is described throughout Ikeda including in Figure 11 and paragraph [0077] in which Ikeda states that "processing in the matrix 20 can be continuously performed by supplying input data to the offchip FPGA 14 and returning the data to the matrix 20 after processing in the FPGA 14." Furthermore, in a search of Ikeda no mention of configuring the FPGA is described. However, Ikeda does not disclose configuring the FPGA in any such manner. Ikeda actually discloses that an advantage of his invention of

configuring a matrix instead of programming the FPGA is "[w]ith this integrated circuit device, there is no need to change all the connections at the transistor level as is the case with an FPGA, so that the hardware can be reconfigured in a short time." (Ikeda, paragraph [0005]). Therefore, the Examiner has mischaracterized Ikeda since Ikeda does not disclose memory storing instructions for a "configuration load function" and a "configuration function" for configuring the FPGA, and in fact describes an advantage of Ikeda's invention is that a matrix is configured instead of the FPGA.

Examiner respectfully traverses Applicant's remark for the following reasons:

Examiner maintains that the Ikeda prior art does disclose the "configuration data", and a memory storing instructions for a "configuration load function" and a "configuration function" for configuring the FPGA as claimed in the pending claims (e.g. claim 1) of the current application. Examiner would like to point out to Applicant that the claimed *configurable logic array* is correctly compared with the Offchip FPGA 14 in Fig. 1 of Ikeda since FPGA is programmable/configurable logic array (see definition in any dictionary). The claim 1 further reads as "a *configurable logic array* having a programmable configuration defined by configuration data stored in electrically programmable configuration points within the configurable logic array". The Ikeda prior art teaches this limitation because the offchip FPGA (14 in Fig. 1) does have programmable configuration (i.e. the offchip FPGA is programmable) defined by configuration data stored in electrically programmable configuration points (i.e. well-

known inherent feature of the FPGA) within the configurable logic array (i.e. 14 in Fig. 1) (e.g. see paragraph [0051] and Fig. 1).

Furthermore, the Ikeda prior art does disclose (i) the claimed "configuration load function" in which the data is loaded/received via the input port from the DRAM 2 in Fig. 1 (e.g. see paragraph [0052] and Fig. 1); and (ii) the claimed "configuration function" in which data is transferred/supplied to the FPGA 14 in Fig. 1 via the data bus 21 in Fig. 1 (e.g. see paragraph [0052] and Fig. 1). Examiner alleges that in paragraph [0051], the Ikeda prior art does disclose about loading/receiving/inputting/outputting data via the input port from/to the external DRAM/device (2 in Fig. 1) to/from matrix (20 in Fig. 1). Even though Ikeda does not specifically recite that the memory (3 in Fig. 1) stores instructions for a configuration load function, the instruction(s) for inputting/outputting data via the input port from/to the external DRAM/device to/from matrix (i.e. the configuration load function) has to be stored in the memory (i.e. the RAM or ROM for storing the execution program 3 shown in Fig. 1) since the matrix is controlled by the instructions/commands from the processor which executes instructions stored in the memory.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Synder (USPN: 7,185,162) discloses the claimed invention, i.e. a flash memory within an IC which loads data from an external memory to an internal

memory and a processor within the IC executes the instruction from the internal memory.

14. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action in this case. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no, however, event will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on 8:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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